New Wave DV

Performance at the Edge

Emerging Trends in HPC

Company Overview

Experts in High-Performance Heterogenous Computing & High-Speed Serial Protocols

Our Mission

Enabling our Partners to Change the World

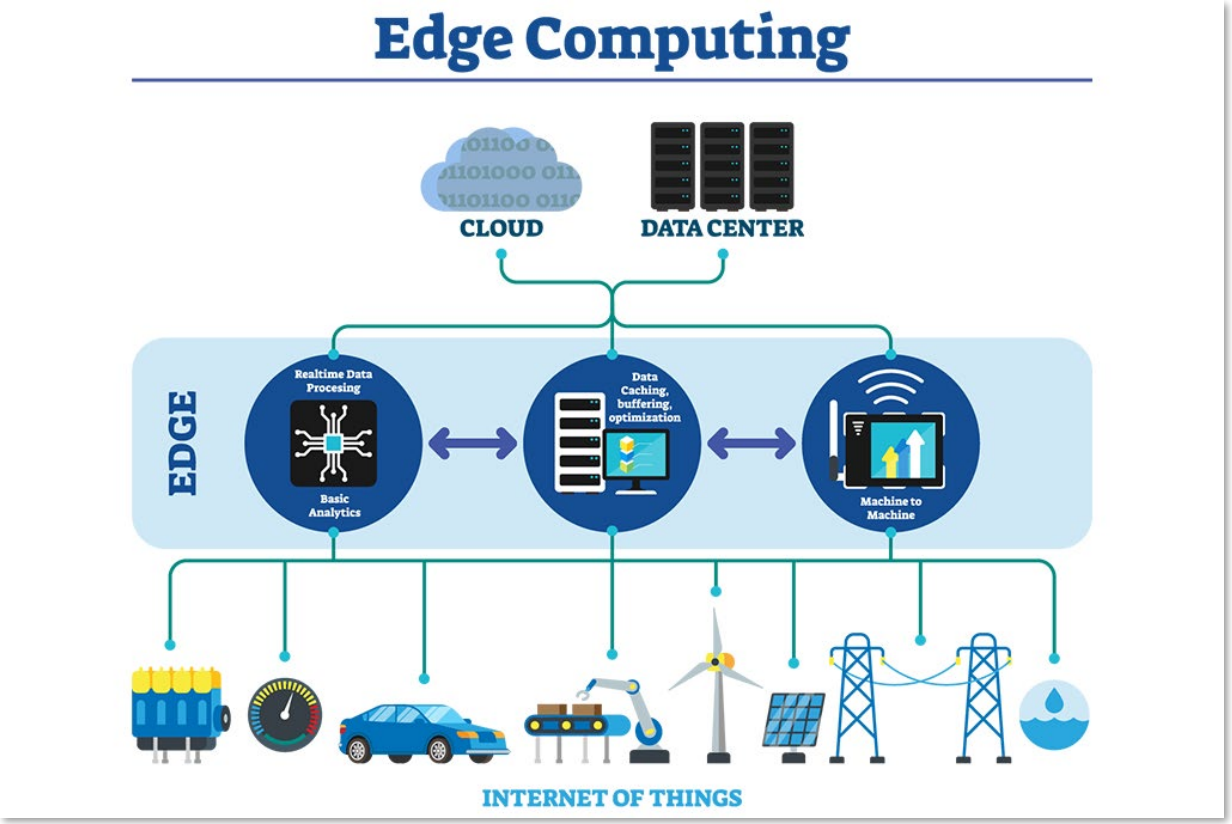
About New Wave DV:

- Headquartered in Eden Prairie, Minnesota
- Core competency is FPGA network engineering
- Local outsourced manufacturing
- ITAR registered
- Strong commitment to customer's support and responsiveness
- Long product life cycle

New Wave DV specializes in:

- Interface Boards
- Intellectual Property
- Hardware Design
- Independent Verification

Performance at the Edge – Emerging Trends in HPC



Edge computing is a distributed computing paradigm that brings computation and data storage closer to the sources of data. This is expected to improve response times and save bandwidth.

Edge computing is an architecture rather than a specific technology, and a topology- and location-sensitive form of distributed computing.

- Wikipedia

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Perspective Matters

From the battle commander point of view, all deployed platforms and sensors are all edge devices.

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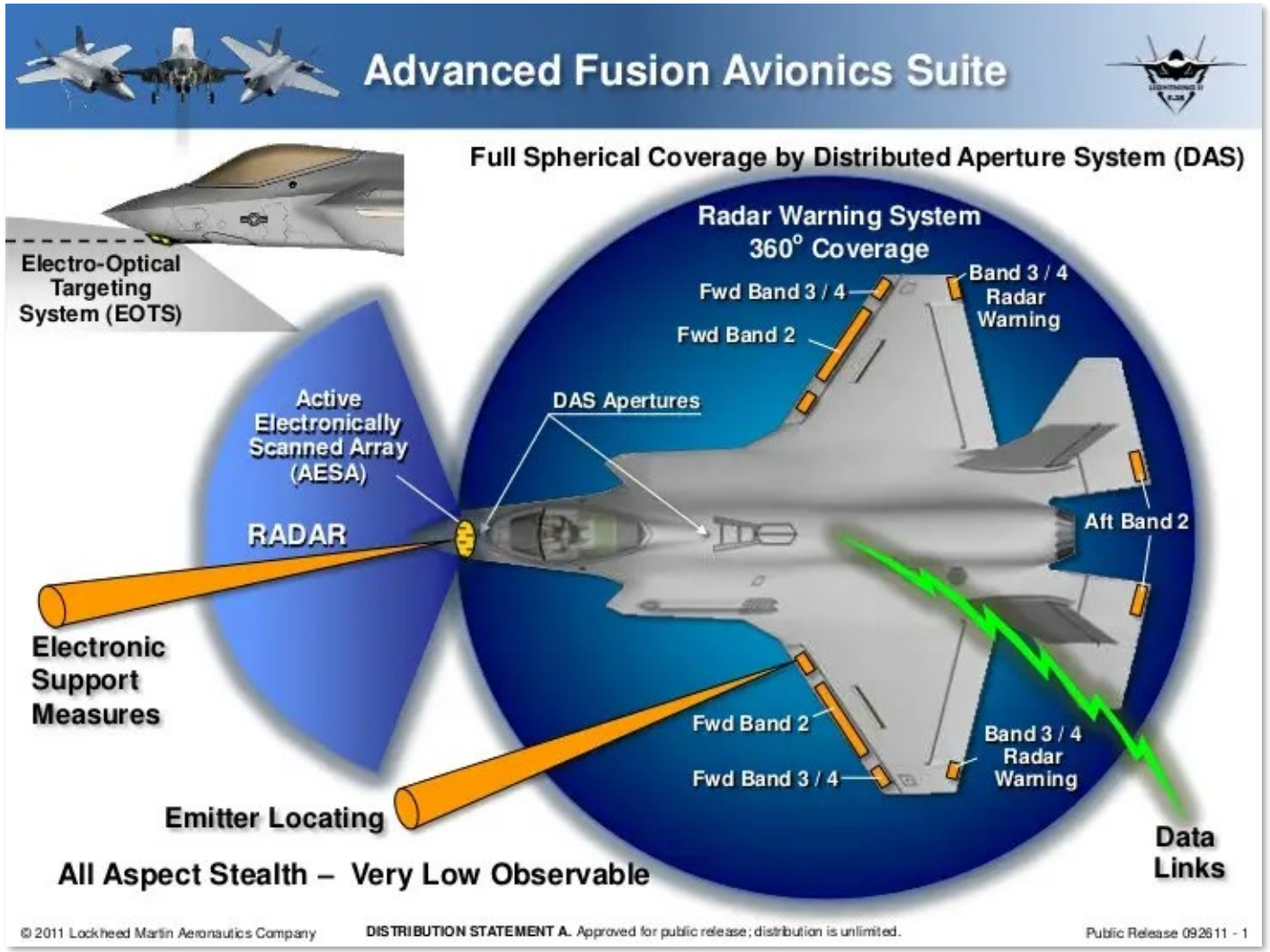

Perspective Matters

Push to the edge says process data as close to the sensor as possible.

However, from an F35 platform perspective (as an example), it is less clear which data should be processed at the sensor aperture vs. processed centrally within the platform. All platforms new and legacy have this same trade-off: XM-30, FVL, NGAD, etc.

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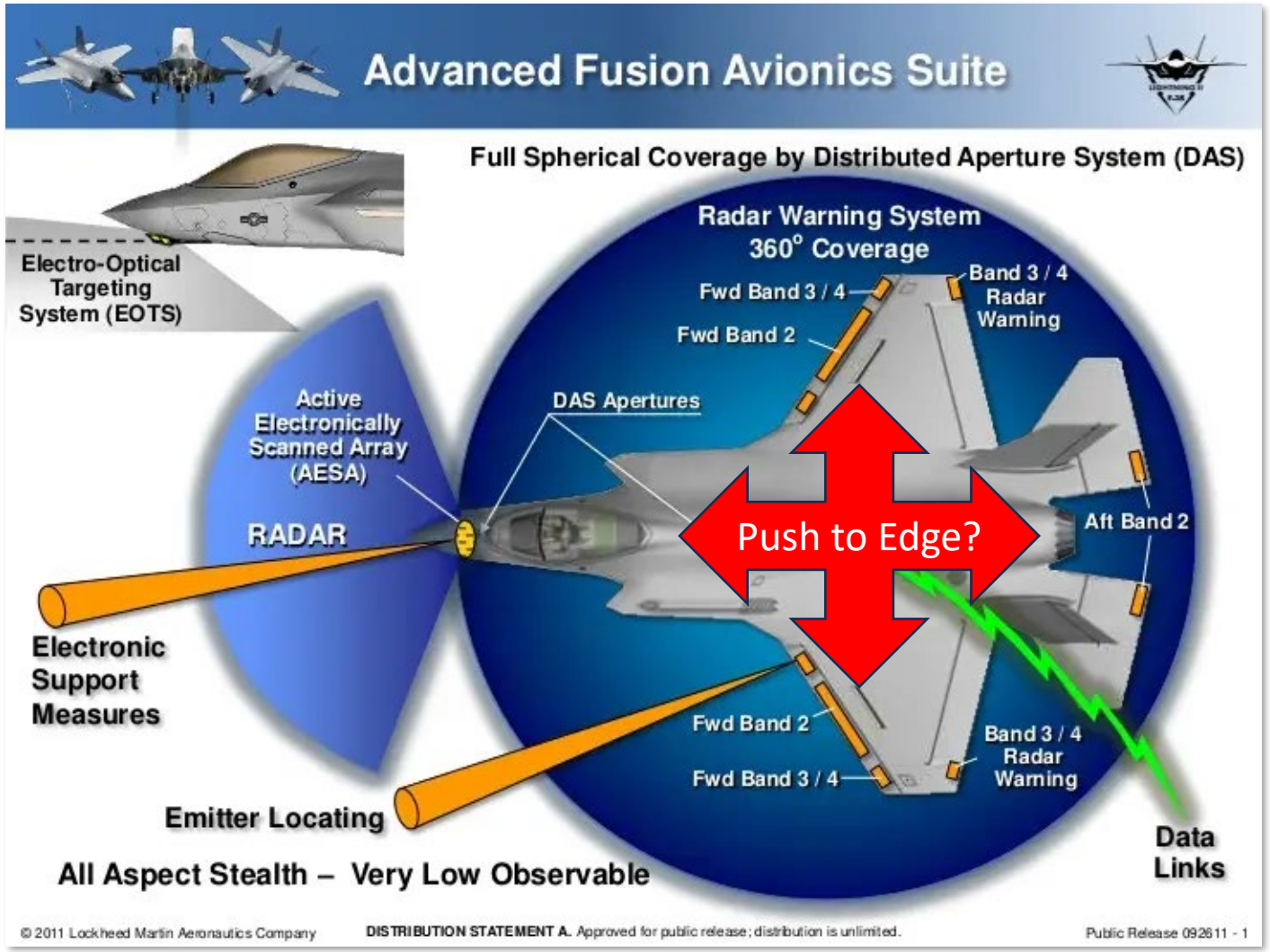

Push Data to the Edge

Difficult Trade-offs:

- New sensors are producing extreme amounts of data, therefore, there are data processing advantages to processing as close to the aperture as possible.

- Real world geometries need considering (EO, DAS, RWR, Countermeasures, etc.) all require multiple sensor apertures on the platform.

- Further, not only does a given domain have multiple sensor apertures, sensor-fusion needs to happen across domains. Multi-function apertures are co-locating domains, but don't solve the geometry.

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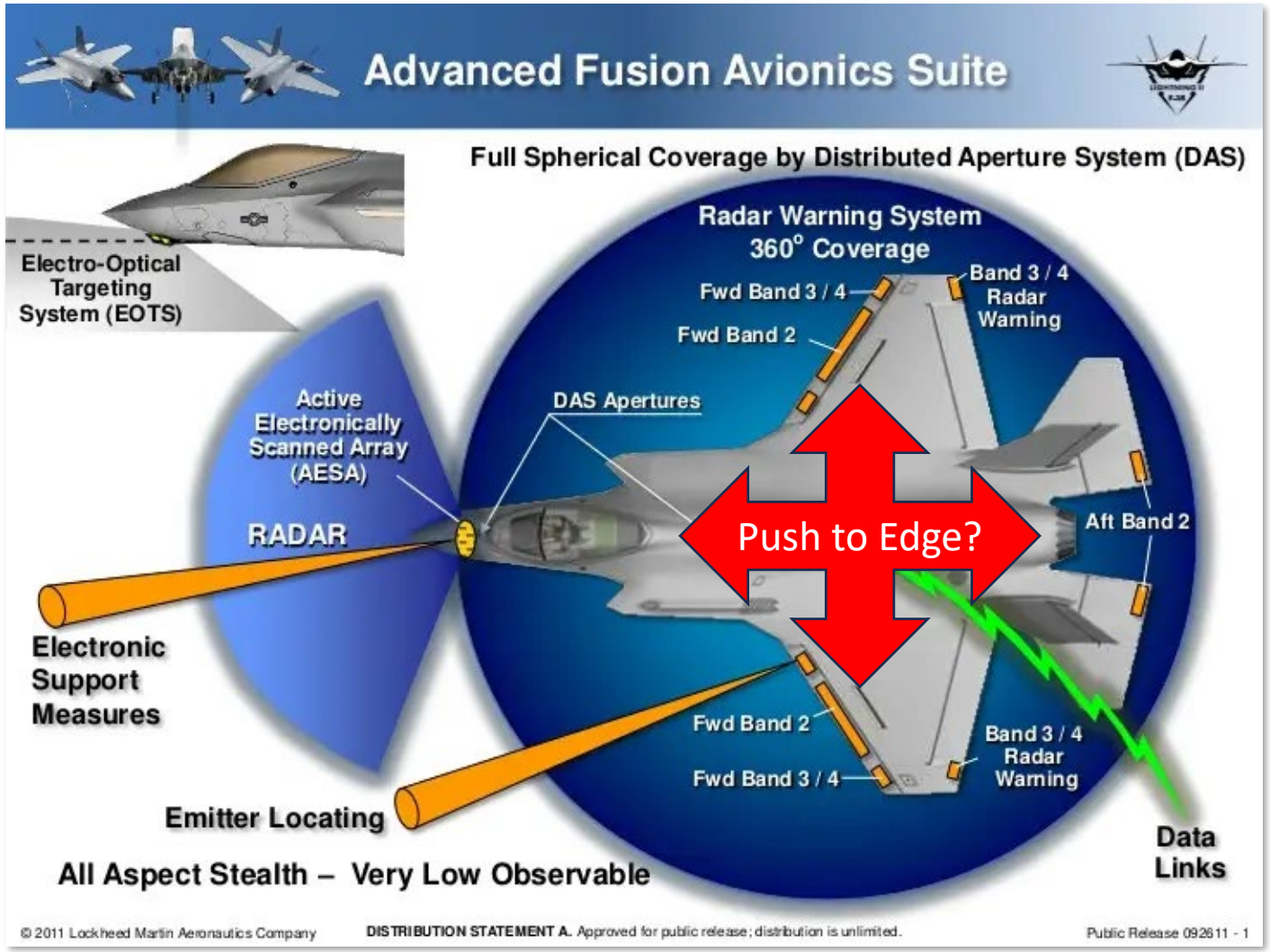

Push Data to the Edge

Competing Requirements:

1. Sensor data growth might push processing further to the edge.
   a) However: AI/ML, heterogenous computing, and future capability preservation thrive when all the data is present, not heavily decimated at the sensor.

2. Need to design and build sensors and processors for future applications, algorithms, AI/ML techniques not known today.

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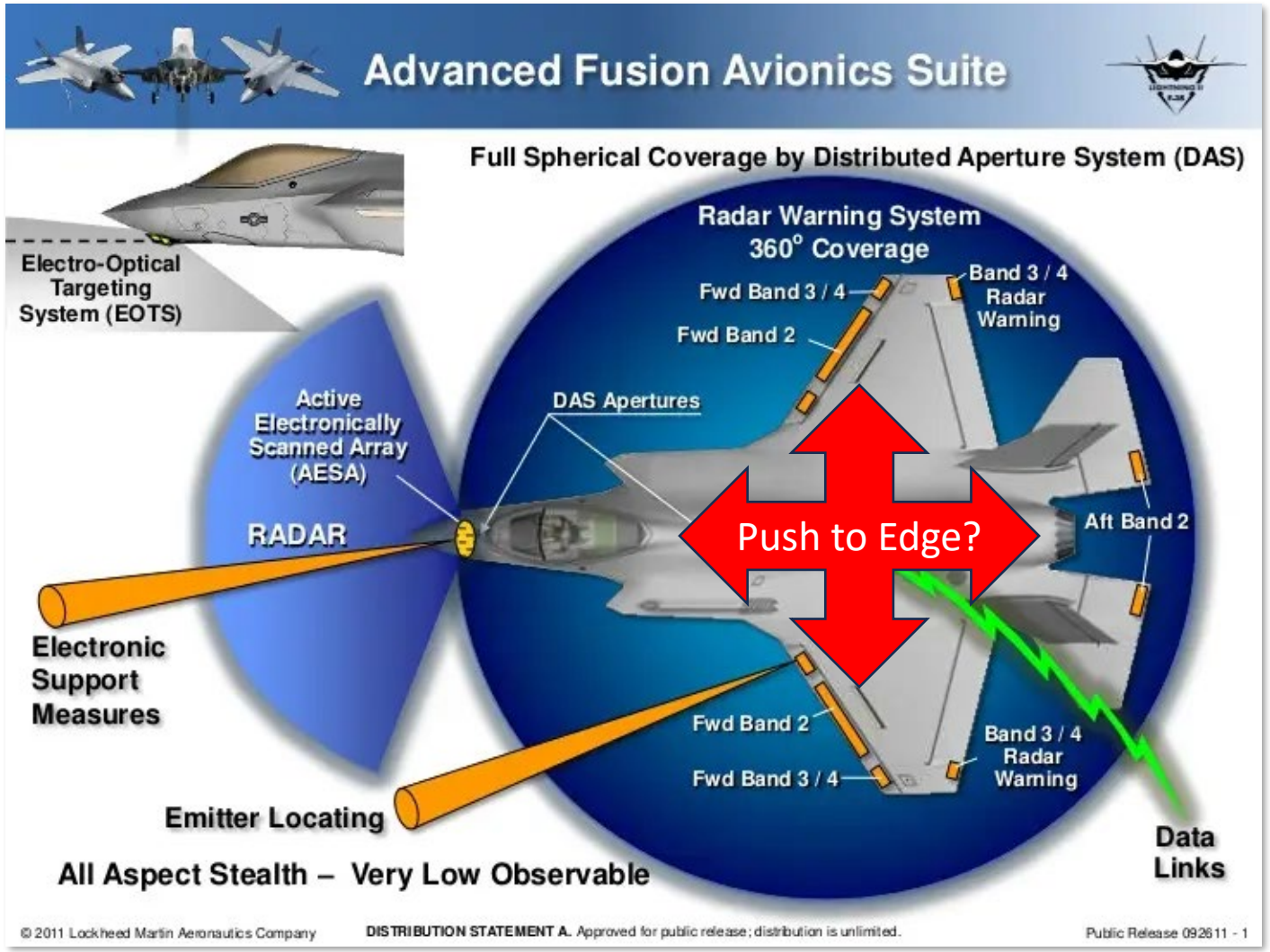

Push Data to the Edge

Competing Requirements:

3. Don't want to remove data that could be used in the future.

4. Dynamics allocation of heterogenous processing elements centrally is more efficient and effective than placing these elements tightly coupled to the sensor.

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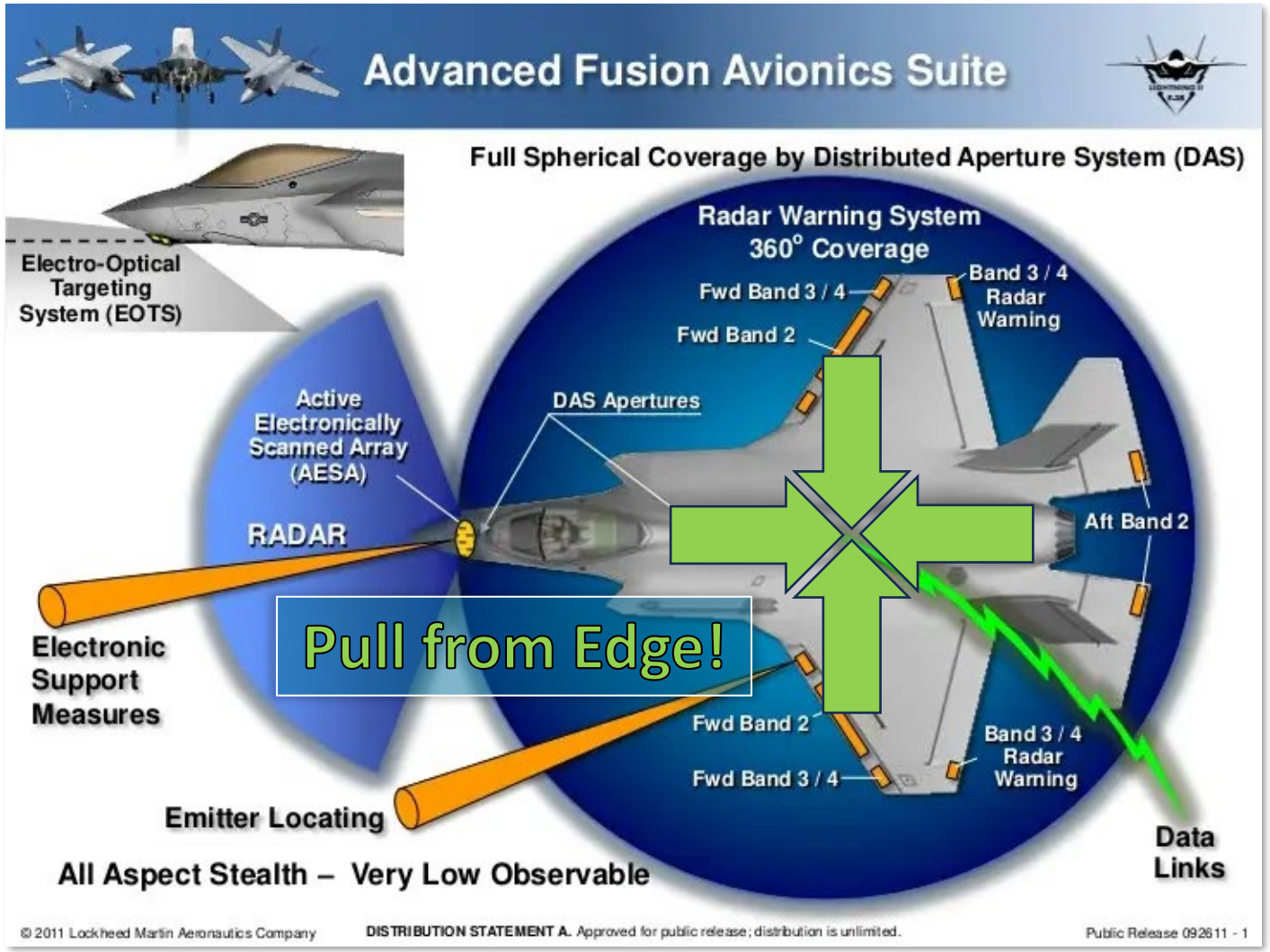

Pull Data From the Edge

Ideal to only digitize at the sensor edge and push all data to centralized sensor fusion processor.

This model enables:

- Dynamic processing allocation across processing elements.
- Sharing of data across individual sensors and sensor domains (EW, EO, Radar, etc.)
- De-coupling of processing hardware and sensor suppliers. Further decoupling of software and algorithm suppliers from hardware vendors.
- Acceleration of AI/ML useability with increased data access

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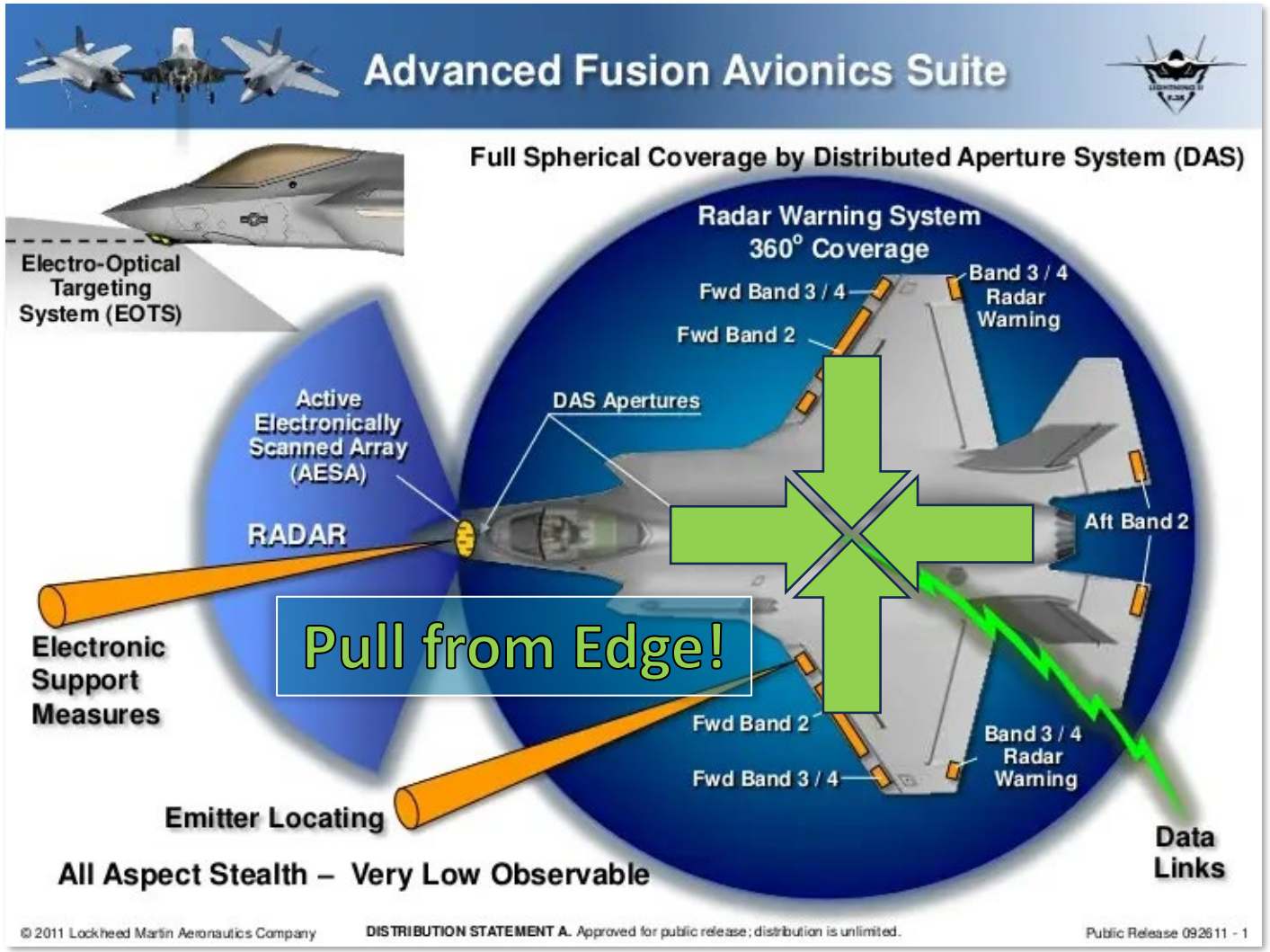

Pull Data From the Edge

Ideal to only digitize at the sensor edge and push all data to centralized sensor fusion processor.

What is needed:

- Very high bandwidth optical network modules and components.

- Essentially the very Edge becomes a “single integrated circuit performing RF to Optics”.

- Rugged extremely high performance and dynamic heterogenous centralized processing.

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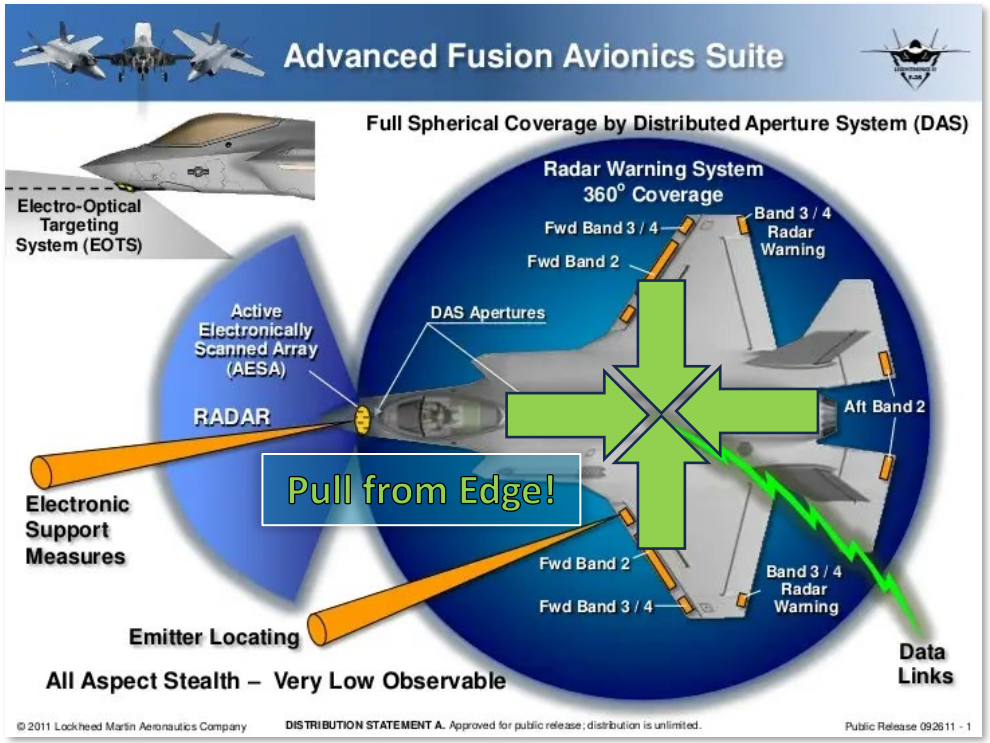
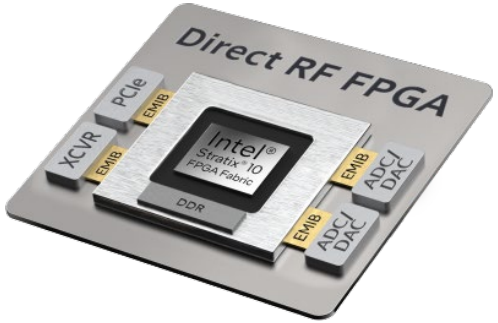
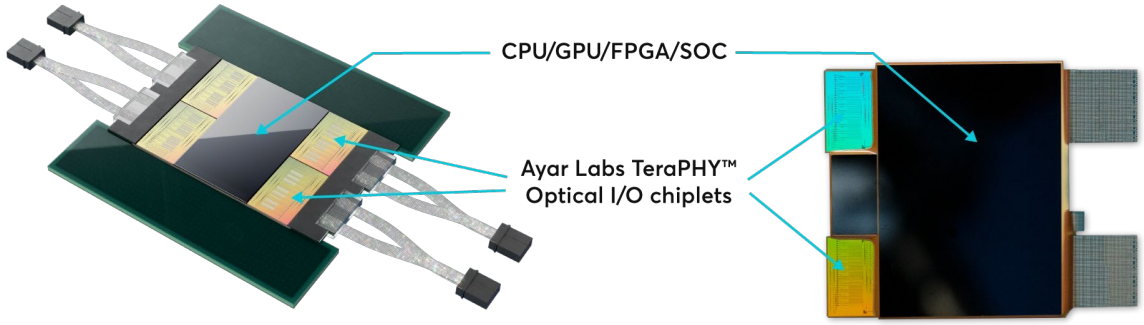


Integrated ADC/DC and Photonics

- To pull from edge, move analog/digital conversion as close to the sensor as possible
- Move as much digitized data between sensors and processors as possible
- Requires improved SWaP near sensors
- Integrated ADC/DAC and integrated photonics make this achievable





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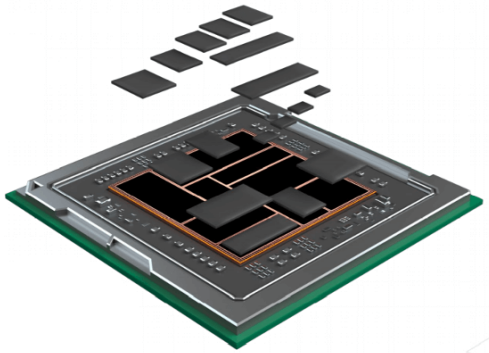


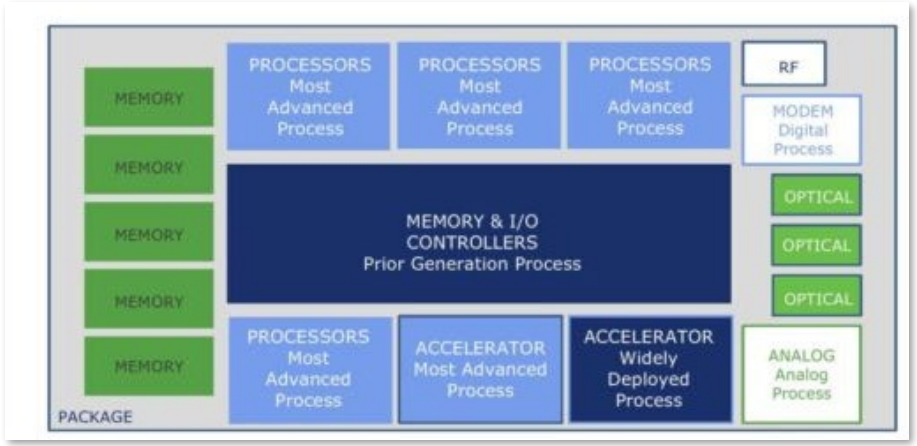
Chiplets

- Enable creation of heterogenous SoCs using best in class silicon

- Reduce area, power, and board complexity

- Provide optimal computing resource for a given workload

- CPUs, FPGAs, GPUs, AI Processors, Memory, ADC/DAC, Photonics in single package



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Interconnects

- Just having “fat pipes” between system resources isn’t enough

- Processing elements in a system need to easily communicate and share data with minimal overhead

- Standards like RoCEv2 provide the ability to move large amounts of data with minimal processor overhead

- CXL provides cache coherent interconnects

- Any element in a compute complex can talk directly over a PCIe fabric to any other element in a system

- UCIe utilizes CXL and PCIe protocols for chiplets to communicate at the package level

CXL Compute Express Link™

UCIe™ Universal Chiplet Interconnect Express

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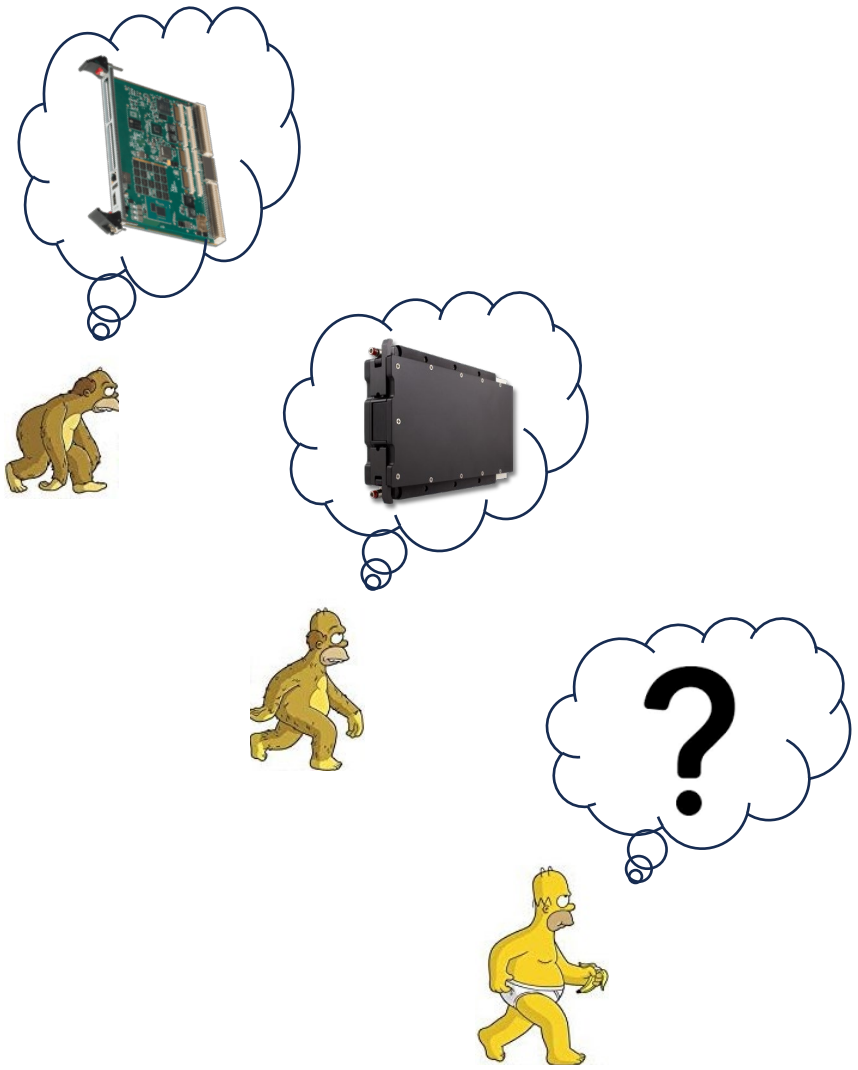


Open Standards Support

- Need open standards that continue to provide the ability to bring best in class high-performance computing capabilities to the embedded world

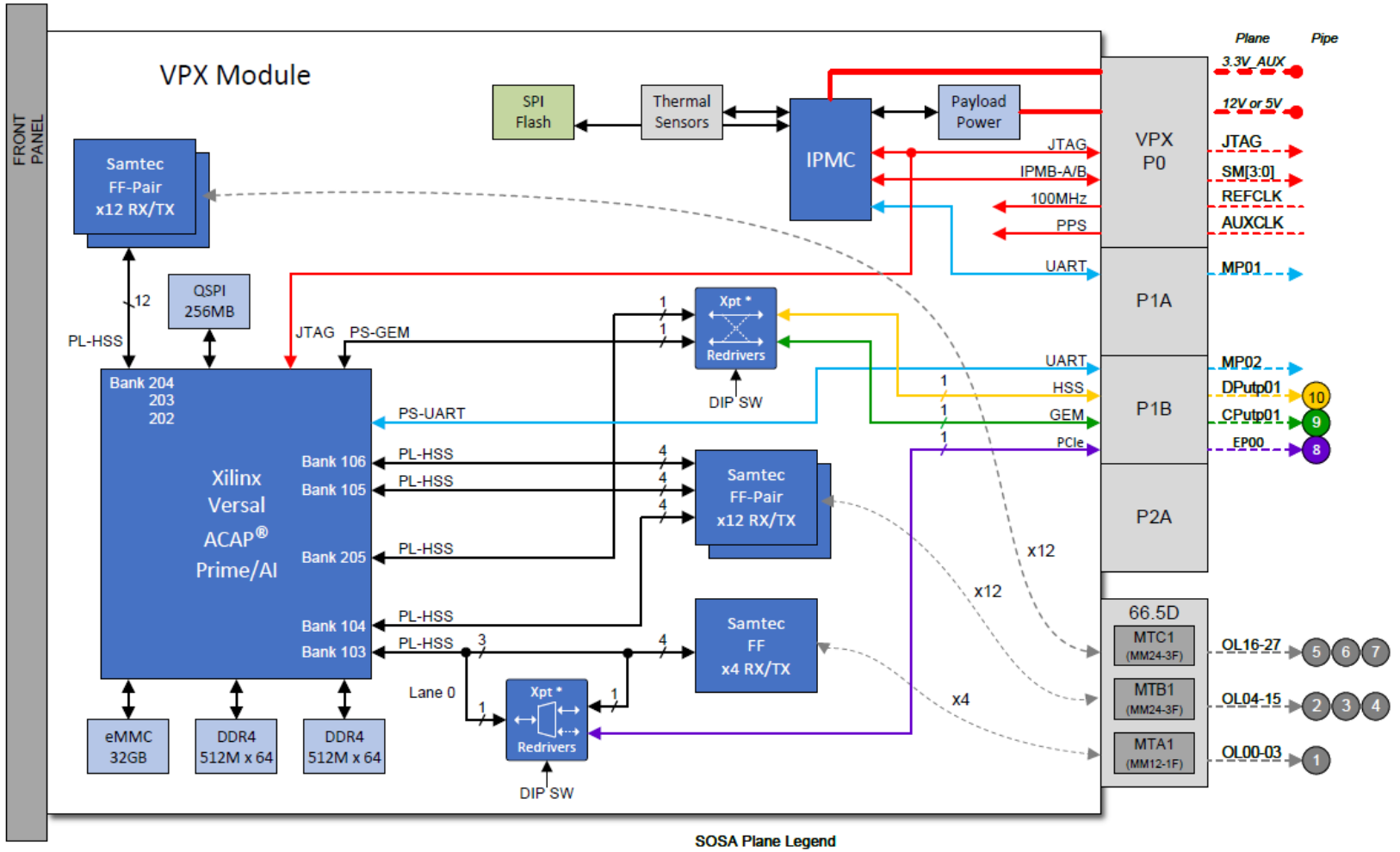
- Enable latest chip technologies, connector technologies, network interconnects, and thermal management techniques

- Enable converged-aperture architectures, sensor fusion, and dynamic reconfiguration of hardware for a variety of mission functions

VITA
Open Standards, Open Markets

SOSA™
Sensor Open Systems Architecture

Example – 700Gbps Optical AI SoC Processor



* Static Physical Layer Cross-Point Switch.
Default through-path for cross-points is shown.
Optional dotted line cross-path indicated. Versal
PL GPIO can be used to override default.

SOSA Plane Legend

CP	Control Plane
DP	Data Plane
EP	Expansion Plane
MP	Maintenance Plane
UP	Utility Plane
OL	Optical Lane

Real World Example:

- Already industry demand for modules supporting 700Gbps optical interface per 3U VPX module.

- Module essentially provides sensor direct to AI/ML Versal FPGA device.

- Same use case(s) expect 5-10x optical density in next-gen architecture.

THANK YOU

New Wave Design & Verification

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